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| 09/932,377 | 08/17/2001 | Steven R. Jahnke | TI-30251 | 4432 |

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| EXAMINER | |
|---|---|
| DANG, KHANH NMN | |

| ART UNIT | PAPER NUMBER |
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| 2111 | |

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Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/932,377 | JAHNKE ET AL. | |
| | Examiner | Art Unit | |
| | Khanh Dang | 2111 | |

*-- Th MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) 1-16 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-16 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Claim Objections*

In claim 1, line 13, "after "bus data." The phrase "capable of supplying device" should be deleted.

### *Claim Rejections - 35 USC § 103*

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Reiss et al in view of Rooney.

At the outset, it is noted that it has been held that the recitation that an element is "capable of" performing a function is not a positive limitation but only requires the ability to so perform. It does not constitute a limitation in any patentable sense. *In re Hutchison*, 69 USPQ 138. In any event, Reiss et al. discloses a data transfer system comprising a plurality of first bus devices, at least one first bus device being a first bus data supplying device (included in PDA 11) capable of supplying data, at least one first bus device being a first bus data receiving device (also included in PDA 11) capable of receiving data and at least one first bus device being a first bus master device (13/or

any master in a multi-master bus) capable of requesting and controlling data transfer; a first data bus (14 or multi-master master bus, see at least col. 5, lines 53-60), connected to each of the plurality of first bus devices and capable of transferring data from a first bus data supplying device to a first bus data receiving device under control of a first bus master device; a plurality of second bus devices, at least one second bus device being a second bus data supplying device ((peripherals, for example) capable of supplying data, at least one second bus device being a second bus data receiving device (memory 21, for example) capable of receiving data, a plurality of second bus devices (17, 23, 25 masters, 33) each being a second bus master device capable of requesting and controlling data transfer; a second data bus (ASB 15) connected to each of said plurality of second bus devices and capable of transferring data from a second bus data supplying device to a second bus data receiving device under control of a second bus master device; a bus bridge (33, for example) connected to the first data bus and the second data bus, the bus bridge (33, for example) capable of supplying data to the first bus, receiving data from said the bus, supplying data to the second bus, receiving data from the second bus, not capable of controlling data transfer on said first bus capable of controlling data transfer on said second bus; a first and a second bus arbiter (it is inherent that separate arbiters must be provided to the first and second buses of Reiss et al., since there are a plurality of devices on the first and second bus accessible to the buses. Arbitration is needed to allow only one device among a plurality of devices to access to a bus based on a predetermined priority scheme) connected to each of the at least one second bus master device, the second bus and the bus bridge, said second

bus arbiter granting control of data transfer on the first bus to one and only one of the set of devices including each second bus master and the bus bridge. However, Reiss et al. does not disclose an address FIFO buffer and a data FIFO buffer, both included in the bus bridge/interface. However, the use of such address and data FIFO buffers is old and well-known in the art as evidenced from at least Rooney. Rooney discloses the use of address and data FIFO buffers (see at least Fig. 2) in a bridge circuit for effectively controlling data flow between two buses having different bus clocks. It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide the bridge circuit of Reiss et al. with address and data FIFO buffers as taught by Rooney for the purpose of effectively controlling data flow in the system of Reiss et al. between two buses having different bus clocks.

Claims 1-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Brooks in view of Rooney.

At the outset, it is noted that it has been held that the recitation that an element is "capable of" performing a function is not a positive limitation but only requires the ability to so perform. It does not constitute a limitation in any patentable sense. *In re Hutchison*, 69 USPQ 138. In any event, Brooks discloses a data transfer system comprising a plurality of first bus devices, at least one first bus device being a first bus data supplying device (RAM, Fig. 1, for example) capable of supplying data, at least one first bus device being a first bus data receiving device (ARM, Fig.1) capable of receiving

data and at least one first bus device being a first bus master device (DMA, Fig.1) capable of requesting and controlling data transfer; a first data bus (AHB or ASB), connected to each of the plurality of first bus devices and capable of transferring data from a first bus data supplying device to a first bus data receiving device under control of a first bus master device; a plurality of second bus devices, at least one second bus device being a second bus data supplying device (peripherals/PIO including external memory via USB, for example) capable of supplying data, at least one second bus device being a second bus data receiving device (data receiving PIO/Timer, Decript, for example) capable of receiving data, a plurality of second bus devices each being a second bus master device capable of requesting and controlling data transfer; a second data bus (APB) connected to each of said plurality of second bus devices and capable of transferring data from a second bus data supplying device to a second bus data receiving device under control of a second bus master device; a bus bridge (201, for example) connected to the first data bus and the second data bus, the bus bridge (201, for example) capable of supplying data to the first bus, receiving data from said the bus, supplying data to the second bus, receiving data from the second bus, not capable of controlling data transfer on said first bus capable of controlling data transfer on said second bus; a first and a second bus arbiter (it is inherent that separate arbiters must be provided to the first and second buses of Brooks, since there are a plurality of devices on the first and second bus accessible to the buses. Arbitration is needed to allow only one device among a plurality of devices to access to a bus based on a predetermined priority scheme)) connected to each of the at least one second bus master device, the

second bus and the bus bridge, said second bus arbiter granting control of data transfer on the first bus to one and only one of the set of devices including each second bus master and the bus bridge. However, Brooks does not disclose an address FIFO buffer and a data FIFO buffer, both included in the bus bridge/interface. However, the use of such address and data FIFO buffers is old and well-known in the art as evidenced from at least Rooney. Rooney discloses the use of address and data FIFO buffers (see at least Fig. 2) in a bridge circuit (including a processor and data/address for effectively controlling data flow between two buses having different bus clocks. It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide the bridge circuit of Brooks with address and data FIFO buffers as taught by Rooney for the purpose of effectively controlling data flow in the system of Brooks between two buses having different bus clocks.

Claims 7-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Brook in view of Rooney as applied to claims 1-6 above, and further in view of the following.

The further difference between Brook and the claimed subject matter is the use of a full bit or empty bit set by the bus bridge to indicate whether the buffers are full or empty; and to generate an interrupt of the processor in the bridge when the address/data buffers are full or empty. It would have been obvious to one of ordinary skill in the art at the time the invention was made to use a full or empty bit set by the bridge in Brook for the purpose of indicating whether the address/data buffers are full or

empty; and to generate an interrupt of the processor in the bridge when the address/data buffers are full or empty, since the Examiner takes Official Notice that the use of a full or empty bit, set by the bridge to indicate whether the address/data buffers are full or empty; and to generate an interrupt of the processor in the bridge when the address/data buffers are full or empty, is old and well-known, and using a full or empty bit, set by the bridge in Brook for the purpose of indicating whether the address/data buffers are full or empty; and to generate an interrupt of the processor in the bridge when the address/data buffers are full or empty, only involves ordinary skill in the art. If Applicants choose to properly challenge the Official Notice, supportive document(s) will be provided upon request.

U.S. Patent Nos. 6,678,756 to Tseng et al., 6,115,760 to Lo et al., 5,678,063 to Odom et al., and 6,477,607 to Jeong are cited as relevant art.

Any inquiry concerning this communication should be directed to Khanh Dang at telephone number 703-308-0211.

Khanh Dang
Primary Examiner